REMARKS

Claims 1-11 are pending in this application. Claim 10 is withdrawn from consideration. By this Amendment, claims 1 and 3 are amended. No new matter is added. Reconsideration of the application is respectfully submitted.

I. Information Disclosure Statement

Information Disclosure Statements with Form PTO-1449 were filed in the above-captioned patent application on October 4, 2005 and October 18, 2005. Applicant has not yet received from the Examiner a copy of the Form PTO-1449 initialed to acknowledge the fact that the Examiner has considered the disclosed information. The Examiner is requested to initial and return to the undersigned a copy of the Form PTO-1449. For the convenience of the Examiner, a copy of each form is attached.

II. Allowable Subject Matter

Applicant gratefully acknowledges that the Office Action indicates that claim 7 includes allowable subject matter.

III. Rejection Under 35 U.S.C. §103(a)

The Office Action rejects claims 1-6, 8, 9 and 11 under 35 U.S.C. §103(a) over U.S. Patent No. 6,812,984 to Watanabe et al. (Watanabe) in view of U.S. Patent No. 5,285,301 to Shirahashi et al. (Shirahashi). Applicant respectfully traverses the rejection.

Watanabe does not teach or suggest an electro-optical device including "at least a part of the identification pattern being formed in the dummy pixel area to overlap with the pixel electrode of the dummy area between the adjacent scanning lines," as recited in independent claim 1.

Watanabe also does not teach or suggest an electro-optical device including "at least a part of the identification pattern being formed in the dummy pixel area to overlap with the

pixel electrode of the dummy area between the adjacent scanning lines," as recited in independent claim 1.

Watanabe shows, in Figs. 1-11, a liquid crystal display including a pixel area P_{ij} and a plurality of address marks, for example, scan address mark 617, provided between an adjacent gate bus line GL_{617} and common electrode line CE_{617}. Although the address marks are formed on the ends of wiring lines, Watanabe does not teach or suggest that pixel electrodes exist in the regions provided between the adjacent gate bus line GL_{617} and the common electrode line CE_{617}. Therefore, Watanabe teaches that the address marks are formed in a non-pixel area that is an area not occupied by pixels P_{ij} and not located between adjacent signal bus lines SL_j or adjacent gate bus lines GL_i. See Fig. 1.

Because pixel electrodes do not exist in the areas where the address marks are formed, the address marks are formed outside of a pixel area. See Figs. 1-11. Therefore, Watanabe cannot reasonably be considered to teach or suggest at least a part of the address marks being formed to overlap with a pixel electrode of a dummy pixel area between the adjacent scanning lines or data lines.

The Office Action acknowledges that Watanabe does not teach or suggest a dummy pixel area. See page 2 of the Office Action. However, the Office Action asserts that Shirahashi remedies the deficiencies of Watanabe. Notwithstanding these assertions, Shirahashi does not teach or suggest an identification pattern that overlaps a pixel electrode of a dummy pixel area located between adjacent signal lines or data lines.

Shirahashi teaches, in Fig. 15, a pixel area of a liquid crystal display having an effective pixel area including transparent pixel electrodes ITO1 and a dummy pixel area including dummy pixel electrodes DITO covered by a light blocking layer BM (hatched area). See col. 13, lines 27-44. Shirahashi also teaches that each of the dummy pixels are connected to, defined by and located between adjacent scanning signal lines GL and adjacent video

signal lines DL. See Fig. 15. Therefore, Shirahashi teaches that the dummy pixels are a part of and formed inside of the pixel area, which is an area located between adjacent scanning signal lines GL and adjacent video signal lines DL. Although the effective pixel area and a dummy pixel area both include pixel electrodes, Shirahashi does not teach or suggest forming an identification pattern in either portion of the pixel area.

Shirahashi also teaches a dummy terminal DGTM of the dummy line DGL disposed outside the outermost scanning signal line GL, and a dummy terminal DDTM of the dummy line DDL disposed outside the outermost video signal line DL of a display matrix. See Fig. 15, and col. 13, lines 30-36. Further, Shirahashi teaches that breakage of the outermost signal lines may be reduced during etching as a result of the structure shown in Fig. 15. See col. 14, lines 15-20. However, Shirahashi does not teach or suggest an identification pattern in either portion of the pixel area.

Even if the pixel area of Watanabe were modified to include the dummy pixel area of Shirahashi, such a modification would locate the dummy pixel area inside of Watanabe's pixel area, that is, located between the adjacent signal bus lines SL_j and the adjacent gate bus lines GL_i. Because the address marks of Watanabe are located in a non-pixel area outside of the pixel area P_{ij}, such a modification would not affect the location of the address marks. Therefore, Watanabe and Shirahashi do not, alone or in permissible combination, teach or suggest the electro-optical panel including at least a part of an identification pattern being formed in a dummy pixel area to overlap with a pixel electrode of the dummy area between adjacent scanning/data lines, as recited in claims 1 and 3, respectively.

For at least these reasons discussed above, claims 1 and 3 would not have been rendered obvious by Watanabe in view of Shirahashi. Claims 2, 4-6, 8, 9 and 11 variously depend from claims 1 and 3, and thus also would not have been rendered obvious by Watanabe in view of Shirahashi, for at least the reasons set forth above, as well as for the

additional features they recite. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-11 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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JAO:HNM/jam

Attachments:
Copy of Form PTO-1449 (filed October 4, 2005)
Copy of Form PTO-1449 (filed October 18, 2005)

Date: December 22, 2005

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